

Appl. No. 10/090,483
Amdt. Dated June 4, 2004
Reply to Office Action of March 4, 2004

Attorney Docket No. 81754.0072
Customer No.: 26021

REMARKS/ARGUMENTS

In response to the Office Action dated March 4, 2004, claims 1, 3, and 5 are amended. Claims 1-15 remain in the application. It is not the Applicants' intent to surrender any equivalents because of the amendments or arguments made herein. Reexamination and reconsideration of the application, as amended, are respectfully requested.

Objections to the Specification

In paragraph 3 of the Office Action, the abstract was objected to because of a typographical error.

The Applicants thank the Examiner and have amended the abstract to overcome the objection. No new matter has been added.

Art-Based Rejections

In paragraphs 4-5 of the Office Action, claims 1-15 were rejected under 35 U.S.C. § 102(e) as being anticipated by Cairns et al., USPN 6,437,767. The Applicant respectfully traverses the rejections, however, in order to expedite prosecution, the Applicants have amended the claims. The Applicants respectfully submit that the claims are patentable in light of the amendments above and the arguments below.

The Cairns Reference

The Cairns reference discloses active matrix devices. FIG. 9 shows a second embodiment of the invention utilising a half-line-at-a-time driving scheme based on split scan lines. In this case each row of pixels within the AMLCD 50 of N rows and

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M columns has two scan lines 51 and 52, the scan line 51 connecting the gates of the TFT's of the left hand group of pixels to a left hand scan line driver circuit 53 and the scan line 52 connecting the gates of the TFT's of the right hand group of pixels to a right hand scan line driver circuit 54. The scan lines 51 and 52 do not overlap so that the pixel aperture ratio is only compromised in the horizontal direction by the width of a single scan line. The two scan line driver circuits 53 and 54 are located at opposite sides of the display and generate signals out of phase with one another by half a line period, the timing of the signals being fundamental to correct operation of the driving scheme. As in the previous embodiment the data line driver circuit 55 comprises a single digital or analogue line memory 56 and line drivers 56A in the form of D/A converters and/or buffers, as will be described in more detail below with reference to FIGS. 11 and 12. See Col. 8, lines 26-45, and FIGS. 9-12.

The Claims are Patentable over the Cited Reference

The claims of the present invention describe a semiconductor integrated circuit that supplies a plurality of display signals to a corresponding plurality of signal electrodes of an image display apparatus. A device in accordance with the present invention comprises a storage device that receives and stores image data, a display signal generation device that generates the plurality of display signals to be supplied to the plurality of signal electrodes based on data stored in the storage device, a first scanning signal generation device that successively generates scanning signals to be supplied to the first group of scanning electrodes based on a clock signal that defines a scanning timing of the image display apparatus, a second scanning signal generation device that successively generates scanning signals to be supplied to the second group of scanning electrodes based on the clock signal, and

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a timing control device that generates the clock signal, and generates a first timing control signal for controlling the first scanning signal generation device and a second timing control signal for controlling the second scanning signal generation device such that the first scanning signal generation device and the second scanning signal generation device generate the scanning signals in a specified order, wherein the first scanning signal generation device outputs a first scanning signal successively to the first group of scanning electrodes based on the first control signal, and wherein the second scanning signal generation device outputs a second scanning signal successively to the second group of scanning electrodes based on the second control signal.

The cited reference does not teach nor suggest the limitations of the claims of the present invention. Specifically, the cited reference does not teach nor suggest at least the limitation of the first scanning signal generation device outputting a first scanning signal successively to the first group of scanning electrodes based on the first control signal, and the second scanning signal generation device outputting a second scanning signal successively to the second group of scanning electrodes based on the second control signal as recited in the claims of the present invention.

The Cairns reference does not use two different signals to control the different scans. As recited in the Office Action, the first timing signal, i.e., SSYNC1, is used as both the first timing control signal and the second timing control signal. The limitation of two control signals as recited in the independent claims is neither taught nor suggested by the Cairns reference.

Each of the independent claims, namely claims 1, 3, and 5, recite that there are two different and distinct signals to control the scanning order and timing.

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Thus, it is submitted that independent claims 1, 3, and 5 are patentable over the cited reference. Claims 2, 4, and 6-15 are also patentable over the cited reference, not only because they contain all of the limitations of the independent claims, but because claims 2, 4, and 6-15 also describe additional novel elements and features that are not described in the prior art.

Conclusion

In view of the foregoing, it is respectfully submitted that the application is in condition for allowance. Reexamination and reconsideration of the application, as amended, are requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles, California telephone number (213) 337-6742 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,
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